REMARKS

This is in response to the non-final Official Action currently outstanding with regard to the present application.

Claims 1-7 and 9-24 were pending in this application at the time of the issuance of the currently outstanding Official Action. By the foregoing Amendment, Applicants have amended Claims 1-3, 5, 7, 9-11, 13, 15, 17, 19-20, and 22-23. No claims are added, canceled or withdrawn. Accordingly, upon the entry to the foregoing Amendment, Claims 1-7 and 9-24 as hereinabove amended will constitute the Claims under active prosecution in this application.

The claims of this application are reproduced above including appropriate status identifiers and showing the Amendments made as required by the Rules.

More particularly, in the currently outstanding Official Action the Examiner has:

1. Acknowledged Applicants' claim for foreign priority under 35 USC §119 (a)-(d) or (f), and confirmed the receipt of the required copies of the priority documents by the United States Patent and Trademark Office;

2. Indicated the drawings filed as part of this application are objected to as not showing every feature of the invention specified in the claims;

3. Acknowledged his consideration of Applicants' Information Disclosure Statements filed in this application on 25 June 2005 and 14 December 2005 by providing the Applicants with a copy of the Forms PTO/SB/08a/b that accompanied those Statements duly signed, dated and initialed to confirm the consideration of the art listed therein – **confirmation of the consideration of the Information Disclosure Statement filed on 25 January 2006 in this application is respectfully requested in response to this communication**;

4. Objected to Claims 2-3, 5, 7, 13, 15 and 17 on the basis of the following alleged informalities:

   In Claim 2 --of the-- must be inserted immediately after "two" in line 8 (as stated in previous amendment), because there is sufficient antecedent basis for this limitation in the claim.

   In Claim 3 --of the--must be inserted immediately after "two" in line 11 (as stated in previous amendment), because there is sufficient antecedent basis for this limitation in the claim and "through" in line 17 (as stated in previous amendment) should be changed to --by--in order to clarify the claimed invention.

   In Claim 5 --and are--should be inserted immediately before "from" in line 4 (as stated in previous amendment) , so as to clarify the first reference voltages are from external first reference voltage supply means and "through" in line 10 (as stated in previous amendment) should be changed to --by-- in order to clarify the claimed invention.

   In Claims 7, 13, 15 and 17 "through" in lines 11, 26, 17 and 18 respectively (as stated in previous amendment), should be changed to --by-- in order to clarify the claimed invention.

5. Rejected Claims 3-7, 13, 14, 17 and 18 under 35 USC § 112, first paragraph, as failing to comply with the written description requirement;

6. Rejected Claims 7, 9-10 and 17-24 under 35 USC § 112, first paragraph, as failing to comply with the enablement requirement;

7. Rejected Claims 7, 9, and 17-21 under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention;

8. Rejected Claims 1-2, 7, 11-12, and 17-18 under 35 USC § 102(b) as being anticipated by Kanatani et al. (US Patent No. 5,414,443) hereinafter "Kanatani", and;

9. Rejected Claims 3-6, 9, 13-16 and 19-21 under 35 USC § 103(a) as being unpatentable over Kanatani, and further in view of Hisashi (JP 10-326084), hereinafter Hisashi.

No further comment regarding items 1 and 3 above is deemed to be required in these Remarks.

With respect to item 2, the Examiner objects to the drawings on the grounds that they do not show each and every feature specified in the claims. In particular, the Examiner asserts that (1) "among power supply voltages supplied to the reference voltage chooser circuit, at least a power supply voltage is supplied to the buffer circuit via a first switch controlled through a first control signal" (Claim 3, lines 14-17 and Claim 13, lines 23-26) is not shown in the drawings, (2) "a reference voltage choosing pattern" as referred to in Claims 7 and 17 is not shown in the drawings; and (3) the two separate decoder circuits referred to in Claims 9, 10, 19 and 20 are not shown in the drawings. The Examiner requires that each of these features be specifically shown in the drawings or that the features not so shown be canceled from the claims.

In response to these objections, Applicants by the foregoing Amendment have modified the phraseology of the various claims at issue such that it now is respectfully submitted to be clear that each and every element being claimed is specifically shown in the drawings as required by the Rules.

More specifically, in Claim 3, Applicants have modified the wording "among power supply voltages supplied to the reference voltage chooser circuit, at least a power supply voltage is supplied to the buffer circuit via a first switch controlled through a first control signal" so as to read -- ~~among power supply voltages supplied to the reference voltage chooser circuit, at least a~~ when a buffer circuit power supply voltage is supplied to the buffer circuit via a first switch controlled through a first control signal--. Similarly, in Claim 13, Applicants have modified the wording "among power supply voltages supplied to the signal line drive circuit, at least a power supply voltage supplied to the buffer circuit is supplied to the buffer circuit via a first switch controlled through a first control signal." so as to read -- ~~among power supply voltages supplied to the signal line drive circuit, at least a~~ a buffer circuit power supply voltage ~~supplied to the buffer circuit~~ is supplied to the buffer circuit via a first switch controlled ~~through~~ by a first control signal.--.

As so amended, Applicants respectfully submit that it now has been made clear in Claims 3 and 13 that there is a distinction between the power supply voltages being applied to the voltage chooser circuit from the power supply voltage being supplied specifically to the buffer circuit(s) via a first switch. Applicants respectfully submit that this feature is clearly shown in Fig. 1 (see also, for example, page 13, lines 17-22). Thus, it will be seen that in Fig. 1 the power supply voltage PW is supplied to the various buffers 37 according to whether or not the control signal CS1 causes the one of the switches 41 associated with each buffer to be open or closed (see, for example, paragraph bridging pages 16 and 17). Accordingly, in view of the foregoing amendments, Applicants respectfully submit that no amendments to the drawings are required to show all of the elements specified in Claims 3 and 13 as hereinabove amended.

Further, by the foregoing Amendment to Claims 7 and 17, Applicants now have clarified that "the reference voltage chosen by the reference voltage chooser circuit changes ~~a reference voltage choosing pattern~~ in response to an output of the decoder circuit". Applicants respectfully submit that this feature is clearly depicted in the upper portion of the circuitry shown in Fig. 1 (see also, for example, pages 25-34). Further, Applicants respectfully submit that this change in the phraseology of Claims 7 and 17 is simply a matter of form that does not change the scope of the claims.

In other words, Applicants respectfully submit that Fig. 1 clearly shows that the output of the decoder circuit determines the reference voltage chosen by the voltage chooser circuit. Of course, the determinations just discussed will clearly define a "pattern" as specifically recognized by the present specification, even though that "pattern" *per se* is not specifically shown in the drawings. Accordingly, Applicants respectfully submit that the amendments to claims 7 and 17 discussed above remove the grounds for the Examiner's objections to the drawings based upon the previous wording thereof and that consequently no amendment of the drawings based upon the Examiner's objections arising from the previous wording of Claims 7 and 17 is required in view of the foregoing amendments. Incidentally in this regard, Applicants respectfully note that by the foregoing amendment the references to a "pattern" that appeared previously in Claims 9, 10 and 19 has been deleted.

The Examiner further has suggested that two **separate** decoder circuits were heretofore defined in Claims 9, 10, 19 and 20. Applicants appreciate the Examiner's close reading of the claims of this application that brought this unintended potential misinterpretation to light. By the foregoing Amendment, Claims 9, 10, 19 and 20 now have been amended so as to distinctly and specifically clarify that only a single decoder circuit is being claimed, the second reference to a decoder circuit in the previous claims being more accurately characterized as a control circuit for changing a decoder table (see, for example, paragraph bridging pages 14 and 15). Accordingly, Applicants respectfully submit that the grounds for the last of the Examiner's objections to the drawings also has been removed by the foregoing Amendment such that no amendment of the drawings based upon the wording of Claims 9, 10, 19 and 20 now should be required.

In summary, Applicants respectfully submit that the amendments just discussed overcome the Examiner's requirement for new drawings. Withdrawal of the currently outstanding requirement for new drawings in response to the currently outstanding Official Action, therefore, is respectfully requested in response to this communication.

Turning now to the Examiner's objections to the claims as summarized in item 4 above, Applicants have reviewed and found the Examiner's proposed changes to the claims to be generally acceptable, with the exception of the change proposed for Claim 2. Accordingly, the foregoing Amendment adopts the Examiner's proposed changes in spirit, although the specific wording of the required changes has been modified slightly for clarity in the foregoing Amendment.

With respect to Claim 2, Applicants cannot agree that there is sufficient antecedent basis for the term "first reference voltage" at the point in the claim referred to by the Examiner. The early part of the claim refers to choosing a "voltage from among reference voltages", but the point in the claim referenced by the Examiner is the first mention of "first reference voltages" as distinct from "second reference voltages". Hence, Applicants respectfully submit that there is no specific antecedent basis for "first reference voltages" earlier in Claim 2 than at the point referenced by the Examiner. Therefore, Applicants respectfully submit that the use of the definite article "the" at the point in the claim suggested by the Examiner is not technically correct.

A decision in response to this communication affirming the accuracy and sufficiency of Applicant's response to the Examiner's objections to the claims, therefore, is respectfully requested.

As summarized in item 5 above, the Examiner has rejected Claims 3-7, 13, 14, 17 and 18 under 35 USC § 112, first paragraph, as failing to comply with the written description requirement.

In this regard, the Examiner first challenges Claims 3, 4, 13 and 14 on the basis that a power supply voltage is not described as being provided to the buffer circuit via a first switch controlled by a first control signal. This is basically the same point discussed above with reference to the Examiner's objections to the drawings. As explained above, by the foregoing Amendment, Applicants have clarified that it is a buffer power supply voltage that is provided to the buffer circuits via a first switch controlled by a first control signal. Applicants respectfully submit that the amendment discussed above on this point also removes the grounds for the Examiner's rejection of Claims 3, 4, 13 and 14 under 35 USC § 112, first paragraph, as failing to comply with the written description requirement. (See, for example, page 13, lines 19-22). A decision so holding in response to this communication is respectfully requested.

The Examiner then challenges Claims 5 and 6 on the grounds that the **voltage divider circuit** does not ***selectively*** provide the second reference voltage to the voltage chooser circuit. In response to the Examiner's rejection, Claim 5 now has been substantially rewritten so as to more accurately reflect the present invention and so as to remove the grounds for the Examiner's rejection under 35 USC 112. Applicants respectfully note in this regard that the fact that the second reference voltage is selectively supplied to the reference voltage chooser circuit via the buffers as controlled by the switches 41 in turn controlled by control signal CS1 is clearly shown in Fig. 1 and described at least at page 13 of the present specification. A decision withdrawing the outstanding rejection of Claims 5 and 6 under 35 USC 112 for failing to satisfy the written description requirement in response to this communication, therefore, is respectfully requested.

Further the Examiner challenges Claims 7, 17 and 18 under 35 USC 112 on the grounds that the specification does not support a decoder table being determined by the number of tones represented by the sampling signal. Applicants respectfully disagree. The present specification discusses this feature of the invention at least at pages 14-15 and 26-31 (See particularly:

Paragraph bridging pages 14 and 15 which states:

> The image signals, fed to the signal line drive circuit 11 for sampling in the sampling and latch circuit 32, are decoded in the decoder circuit 33 in the succeeding stage to produce signals controlling the reference voltage chooser circuits 34. The decoder circuit 33 can change the decoder table before actually using the decoder table for decoding. This function will hereinafter be referred to as variable decoding. The changing of the decoder table is controlled by the third control signal CS3 supplied from the setup circuit 14.

Page 29, lines 5-8, which states:

> "Table 2, when compared with Table 1, shows the switching between conversion schema by means of decoder tables ***so that the conversion matches the number of tones represented by the image signals***." (Emphasis added), and

to the same effect, page 31, lines 4-7, which state:

> "Table 3, when compared to Tables 1 and 2, again shows the switching between conversion schema by means of decoder tables ***so that the conversion matches the number of tones represented by the image signals."*** (Emphasis added)

Still further, the final paragraph on page 77 and the first paragraph of page 78 the present specification read as follows:

> In the image display device, the control means may control the switching between the decoder tables according to the number of tones represented by the image signal.
> In the arrangement, the control means controls the switching between the decoder tables according to the number of tones represented by the image signal. This allows arbitrary selection of the level of power saving in the image display device in line with operating conditions.

Applicants respectfully submit that these representative passages of the present specification constitute a significant part of the clear and complete disclosure of the point that the Examiner has alleged was not disclosed in the present specification, i.e., that the decoder tables are determined by the number of tones represented by the sampling signal. Accordingly, the withdrawal of the Examiner's rejection of Claims 7, 17 and 18 based upon an alleged failure to satisfy the written description requirement is respectfully requested in response to this communication.

As summarized in item 6 above, the Examiner also alleges in the currently outstanding Official Action that Claims 7, 9, 10 and 17-24 are not enabled by the present specification. Again Applicants respectfully disagree.

By the foregoing Amendment, Applicants have amended Claims 7 and 17 as follows for clarity:

> the decoder circuit is controlled ~~through~~ by a third control signal
> according to a decoder table determined by the number of tones represented by the sampling signal; and
> the reference voltage chosen by the reference voltage chooser circuit
> changes ~~a reference voltage choosing pattern~~ in response to an output of the decoder circuit

Hence, Applicants respectfully submit that the concept of the decoder circuit causing the reference voltage selected by the voltage chooser circuit to change is clearly disclosed in the specification (see Page 26 et seq.) in a manner that would allow one skilled in the art to practice the present invention without the need for extensive or inappropriate experimentation. Applicants therefore respectfully submit that the foregoing Amendment removes the grounds for the Examiner's outstanding enablement rejection, i.e., that the reference voltage chooser circuit is not capable of changing the reference voltage choosing pattern. In other words, as has been referred to extensively above, the decoder circuit can change the decoding table, and the change of the decoder table in turn causes the voltages chosen by the voltage chooser circuit to change. (see, for example, page 26, lines 4-12) Accordingly, Applicants respectfully submit that as above amended Claims 7, 17 and 18 are clearly enabled by the present specification. Withdrawal of the currently outstanding rejection of Claims 7, 17 and 18 on the grounds of a failure to present an enabling disclosure, therefore, is respectfully requested in response to this communication.

The Examiner's rejection of Claims 9, 10 and 19-24 on the basis of a failure to present an enabling disclosure of separate decoder circuits has been discussed and disposed of above with regard to Applicants amendments of the claims so as to remove any necessity for the amendment of the drawings to show the multiple decoder circuits allegedly claimed. In short, to the extent that separate decoder circuits conceivably might have been read as being specified by the previous claim language, that misconception has been removed by the foregoing Amendment.

Still further, with regard to the signal line drive circuit operation that the Examiner alleges not to be adequately disclosed, Applicants again respectfully call attention at least to pages 21-46 of the present specification wherein the setup circuit and the operation of the present invention in numerous modes are set forth using one or more of each of the alternatives claimed.

Applicants respectfully submit, therefore, that the Examiner's rejections based upon an alleged lack of enablement in the present specification have been overcome by amendment, or demonstrated to be in error, by the foregoing discussion. Accordingly, a decision withdrawing the currently outstanding enablement rejections in response to this communication is respectfully requested.

As summarized in item 7 above, the Examiner rejects Claims 7, 9, and 17-21 under 35 USC 112 as being indefinite. By the foregoing Amendment, the alternative phraseology "and/or" and "closure/opening" has been removed from the Claims in favor of more precise phraseology. Hence, Applicants respectfully submit that the currently outstanding rejections of Claims 9 and 19-21 on indefiniteness grounds have been removed by the foregoing Amendment.

As to Claims 7, 17 and 18, the Examiner's attention respectfully is directed to page 26 of the present specification whereat it is stated:

> The decoder circuit 33 of the present invention differs from decoder circuit 114 (prior art) in that the decoder circuit 33 can change the conversion scheme of the sampling data to the control signal through the third control signal CS3. Specifically, the decoder circuit 33 includes an arrangement to switch between decoder tables for use in signal conversion through the third signal CS3 (variable decoding).

Accordingly, it will be understood that the decoder circuit is controlled by a third control signal according to a decoder table. In other words, the decoder circuit is controlled by the third control signal so as to operate according to a particular one of the decoder tables (such as Tables 1-3 as set forth in the present specification). Applicants respectfully submit that this feature of the present invention is appropriately clearly and distinctly phrased in the claims as they presently stand, particularly when the claims are read in light of the specification as they are supposed to be read.

With regard to the currently outstanding rejections under 35 USC 112, therefore, Applicants agree with the Examiner to the extent that some of the wording of the claims of this application prior to the foregoing Amendment may have been somewhat unclear and/or subject to misinterpretation. In those respects, the claims of this application now have been thoroughly reviewed and revised so as to remove any unclear phraseology and/or the chance that the claims might be misinterpreted Applicants believe, however, that the Examiner's rejections for failure to comply with the written description requirement, failure of the specification to provide an enabling disclosure, and/or failure to distinctly point out and particularly claim the subject matter regarded as the invention in the currently outstanding Official Action all arise from factors that have been corrected by the foregoing Amendment Accordingly, reconsideration and withdrawal of the currently outstanding rejections under 35 USC 112 in view of the foregoing Amendment and Remarks are respectfully requested in response to this communication.

Turning now to the Examiner's substantive rejections as summarized in items 8 and 9 above, the Examiner has rejected claims 1-2, 7, 11-12, and 17-18 under 35 USC §102(b) as being anticipated by Kanatani et al. (US 5,414,443). In addition, the Examiner has rejected claims 3-6, 9, 13-16 and 19-21 under 35 U.S.C. §103(a) as being unpatentable over Kanatani in view of Hisashi (JP 10-326084, see English translation attached to outstanding Official Action).

More specifically, the Examiner suggests that the Kanatani reference discloses the present invention as currently claimed in Claims 1, 2, 7, 11, 12, 17 and 19. Hence, the Examiner suggests that the Kanatani et al reference discloses "reference voltage transmission means for ***directly*** transmitting ***the first reference voltages (VCC and VDD)***" to a voltage chooser circuit indicated at 55 (Fig. 7) from external voltage supply means. Applicants do not entirely disagree.

It is to be noted in the latter regard that the Examiner's position fails to take note of the fact that in the Kanatani et al reference, the positive and negative voltage signal output circuits 70 and 74 (that are respectively responsible for the transmission of VCC and VDD) are activated ***alternatively*** in accordance with the output from the selector circuit 79 so as to provide voltage outputs via analog gates $72_0 - 72_7$ ***or*** $76_0 - 76_7$. This mode of operation is explained in detail in the Kanatani et al reference at Column 10, line 33 through Column 12, line 29 (particularly Column 11, line 37 to Column 12, line 29) and with respect to a different embodiment at Column 14, lines 27-53. These portions of the Kanatani et al reference clearly and specifically disclose that reference voltages VCC ($= +V_7$) and VDD ($= -V7$) (i.e., first reference voltages provided from external) are provided to the voltage chooser circuit via analog gates 72_7 and 76_7, respectively, according to the control signals provided by the selector circuit 79.

Consequently, Applicants respectfully submit that it is clear that the Kanatani et al reference does not teach, disclose or suggest that ***multiple*** first reference voltages are to be provided ***directly*** (as opposed to via a controlled switch) to the voltage chooser circuit ***simultaneously*** (rather than alternatively according to which portion of the circuit is activated at any specific time by control circuit 79). At best, therefore, in Kanatani, et al. VCC is provided directly to the voltage chooser circuit via analog gate 72_7 when the circuit 7 is in one condition, and the voltage VDD is provided directly to the voltage chooser circuit via analog gate 76_7 when the circuit 7 is in its alternative condition. Therefore, there is no time during which ***multiple*** first reference voltages are provided to the voltage chooser circuit ***at the same time*** as is the case in the present invention. Further, it is to be noted that the reference voltage V_c is not provided to the voltage chooser circuit 55 at all.

Accordingly, it will be understood that the Kanatani et al reference indicates that in the drive circuit as shown in Fig. 7 the "power supply voltages VCC, VDD" from external are controlled by the output of the "non-inverting level shifter 794" or the "inverting level shifter 795" in the "selector circuit 79" when they are fed to the "voltage level chooser circuit 55". However, the "voltage level chooser circuit 55" does not directly receive both of the "power supply voltages VCC, VDD" (i.e., the first reference voltages) and the voltage signals V_0 to $+V_6$ or V_0 to $-V_6$ (i.e., the "second reference voltages") obtained by voltage division of the "power supply voltages VCC or VDD" ***simultaneously***. Hence, the Kanatani et al arrangement lacks the features of the present invention that allow the benefit of reduced buffer power consumption without adverse affect on the display.

In other words, in the signal line drive circuit and image display device of the present invention, the reference voltage chooser circuit receives not only the second reference voltage obtained by dividing at least two of the multiple first reference voltages, but also ***simultaneously and directly*** receives the multiple first reference voltages themselves. Hence, the reference voltage chooser circuit ***directly*** receives the multiple first reference voltages and the selected ones of the second reference voltages obtained by dividing at least two of the multiple first reference voltages ***at the same time***. Consequently, the signal line drive circuit and image display device of the present invention includes not only voltage lines for feeding the second reference voltages obtained by dividing at least two of the multiple first reference voltages to the reference voltage chooser circuit via buffers, but also reference voltage lines for directly feeding the multiple first reference voltages to the reference voltage chooser circuit ***simultaneously***. Thus, even if, for example, the first switch is turned off to cut power supply voltage to all of the buffer circuits, the display will remain unaffected while the current consumption (power consumption) of the buffer circuits will be reduced. (see present specification at page 17, lines 12-24 and Fig. 1). Such clearly and definitely is not the case in the Kanatani et al reference.

Further, it will be understood that the same arguments that were presented in the last amendment filed in this application with respect to the Hasihi reference apply to the Kanatani et al reference. ***Indeed, the Kanatani et al reference simply represents the embodiment of the Hasishi reference discussed in the last amendment in this application that could only be achieved by the assumption that a first reference voltage passed directly through one of the buffers therein disclosed.*** The fact that the Examiner has found a reference that does not require the conjecture applied with respect to Hasishi previously does not alter the conclusion that the presently cited references ***do not teach, disclose or suggest the provision of multiple first as well as second reference voltages to the voltage chooser circuit simultaneously***.

Accordingly, it will be recalled that the present invention has the objectives of reducing power consumption in a signal line drive circuit without adverse impact upon the operating characteristics thereof; providing an image display device that utilizes that signal line drive circuit; and providing portable apparatus utilizing that signal line drive circuit. Further, Applicants have noted that to accomplish these objectives the present invention (i) eliminates an unnecessary circuit from prior art configurations, (ii) eliminates the current that would otherwise be used in the eliminated circuit, and (iii) avoids the occurrence of charging/discharging stray capacitance between bus lines when the image signal represents a small number of tones. These objectives and the manner of their accomplishment is not taught, disclosed or suggested by the Kanatani et al reference or the Hasishi et al reference taken either alone or in combination with one another.

An important technical difference between the present invention and the Hisashi reference lies in ***whether or not multiple first reference voltages from external first reference voltage supply means are provided directly to the reference voltage chooser circuit.*** In the present invention multiple first reference voltages are provided ***directly*** to the voltage chooser circuit from external first reference voltage supply means, but that in the Hisashi reference this is not the case. The reason for this lies in the difference between the techniques utilized by Hisashi and the present invention in the determination of which image tones are to be displayed (i.e., functional considerations not directly pertinent to the differences in structure between the present claims and the cited art) and in the ability of the present invention to avoid deterioration of the image to be displayed.

Accordingly, Applicants again respectfully emphasize that in the signal line drive circuit and image display device according to the present invention, the reference voltage chooser circuit is capable of ***simultaneously*** receiving not only (i) the second reference voltages obtained by dividing the first reference voltages via buffers, but also (ii) ***multiple*** first reference voltages **directly from** the external first reference voltage supply means. In other words, the reference voltage chooser circuit of the present invention can receive two different types of reference voltages in two different ways ***simultaneously***. The multiple first reference voltages each are provided directly from the external first reference voltage supply means to the voltage chooser circuit, and the second reference voltages created by voltage division from the first reference voltages are provided to the reference chooser circuit via buffers.

In Hisashi, on the other hand, no first reference voltage is provided **directly** to the voltage chooser circuit. Instead, ***a single*** first reference voltage VDD2 is provided to the voltage chooser circuit via a buffer as the voltage Vo and second reference voltages V1-V15 created by voltage division between VDD2 and ground also are provided to the voltage chooser circuit via buffers (i.e., the structure of the Hisashi reference includes buffers that respectively correspond to ***all*** of the tones of the sampled image, see, Hisashi at Claim 1, lines 3-4). Hence, as is the case with respect to the Kanatani reference, Applicants respectfully submit that the Hisashi reference also fails to teach, disclose or suggest ***multiple*** first reference voltages provided ***directly*** to the voltage chooser circuit.

In other words, even if one assumes a total pass though by the Hisashi buffers when the switches associated with the buffers are activated by VSYNC (12), the Hisashi reference teaches, discloses or suggests only a single first reference voltage from an external reference voltage supply means provided to the voltage chooser circuit via the buffer associated with SW0 in Hisashi's Fig. 3 just as Kanatani et al teaches the pass though of either VCC or VDD alternately, not together.

As mentioned above, according to the present invention, the first reference voltages supplied continuously to the voltage chooser circuit portion of the signal line drive circuit prevent the deterioration of display quality even when the first switch is OFF such that no power voltage is supplied to the buffers. This allows a reduction in the current consumption (power consumption) in the buffers. (See, page 17, lines 12-24, and Fig. 1 of the present specification). In the Hisashi device, on the other hand, the voltage chooser circuit receives input voltage only while the switch is ON. When the switch is OFF, the application of voltage, including the constant voltage VDD2, to the buffers is cut off with the result that the buffers stop operating and substantially no bias current flows therethrough. (See, Hisashi at paragraph 0009, lines 28-31) Accordingly, when the current consumption (power consumption) in the buffers is reduced in the Hisashi reference by turning the switch OFF, there is an inevitable deterioration in the quality of the display unlike the situation with respect to the present invention. Consequently, one skilled in the art would not be led to combine the Kanatani et al reference with the Hisashi et al reference in order to achieve the goals of the present invention, and even if that combination were to be made it would be unsuccessful for the intended purpose.

In addition, with specific regard to Claims 7 and 17, Applicants respectfully note that by adopting the structures herein claimed the number of bus lines to which the image signal is supplied can be reduced. This also allows for the reduction of the power required by the device (i.e., reduces power consumption) according to the number of tones required for the transmission of the data via the bus lines.

Also as stated previously, a main feature of Claim 7 is that ***a decoder circuit*** controlling the reference voltage chooser circuit ***is controlled through a third control signal to change a decoder table determined by the number of tones represented by a sampling signal generated by a sampling of the image signal***, whereby the reference voltage chooser circuit changes a reference voltage choosing pattern of the signal line driving circuit. Claim 17 incorporates these features into the display device therein claimed. In either case, however, it will be understood that as emphasized above with regard to the Examiner's enablement and written description rejections, in the present invention the decoder table used can be changed in accordance with the number of tones represented by the image signal. Consequently, the signals transmitted by the bus lines may be fixed when the image signal represents a small number of tones. This fixation prevents the occurrence of the charging/discharging of stray capacitances between the bus lines thereby also reducing the power consumption of the signal line driving circuit. This feature also is neither taught, disclosed nor suggested by either the Kanatani et al reference, or the Hisashi et al reference, or any combination thereof.

More particularly, conventionally in cases where for example 6 bus lines are provided (i.e., a 6 bit mode), signals indicative of "1" and "0" need to be supplied to all six bus lines so as to express "white" or "black". In cases wherein 6 bus lines are provided in the context of the present invention as claimed in Claims 7 and 17, however, a signal indicative of "1" or "0" has to be supplied to only one bus line so as to express "white" or "black" while the signals supplied to the other bus lines can remain fixed to "0" or "1". Neither the Kanatani et al nor the Hisashi reference, teach, disclose or suggest a structure for "reducing the number of bus lines to which the image signal is supplied or a structure for reducing power consumption equivalent to that presently claimed in Claims 7 and 17.

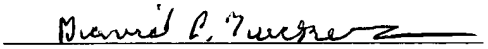
Therefore, it will be understood that a main feature of the present invention is that the claimed structure includes reference voltage supply means ***directly*** inputting (i.e., directly transmitting without the intervention of other circuit elements) ***multiple*** first reference voltages supplied by external first reference voltage supply means to a reference voltage chooser circuit. With that arrangement, no buffer circuit is required for the reference voltage line(s) directly transmitting the first reference voltages. Therefore, the signal line drive circuit takes up a smaller area and eliminates the amount of current that would otherwise be utilized by buffer circuits associated respectively with the first reference voltages. This results in power savings by the claimed signal line drive circuit in comparison to the prior art. In addition, when second reference voltages are provided to the voltage chooser circuit via buffers, those second reference voltages are provided to the voltage chooser circuit ***simultaneously*** with the first references voltages whereby the voltage chooser circuit can effectively choose among them according to the decoder table then in use.

For each and all of the foregoing reasons, Applicants respectfully submit that the claims of this application as they will stand upon the entry of the foregoing Amendment now are in condition for allowance. Therefore, reconsideration and allowance of this application in view of the foregoing Amendment and Remarks is respectfully requested in response to this communication.

Applicant also believes that additional fees beyond those submitted herewith are not required in connection with the consideration of this response to the currently outstanding Official Action. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge and/or credit Deposit Account No. 04-1105, as necessary, for the correct payment of all fees which may be due in connection with the filing and consideration of this communication.

Respectfully submitted,

Date: April 25, 2006



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